FIG.1

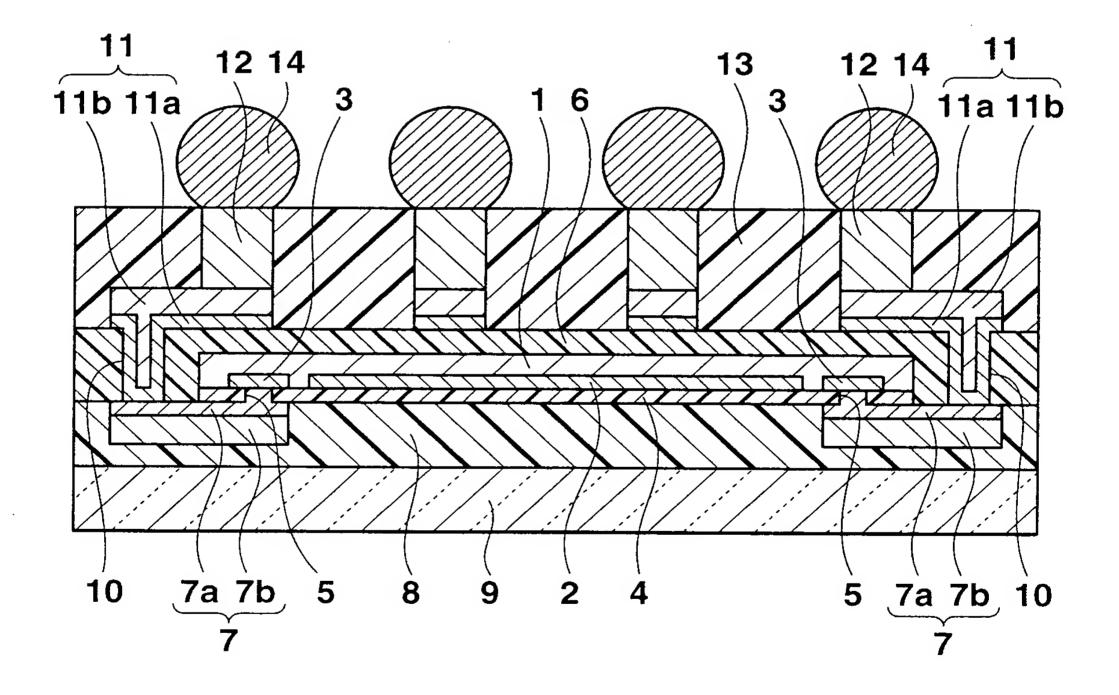
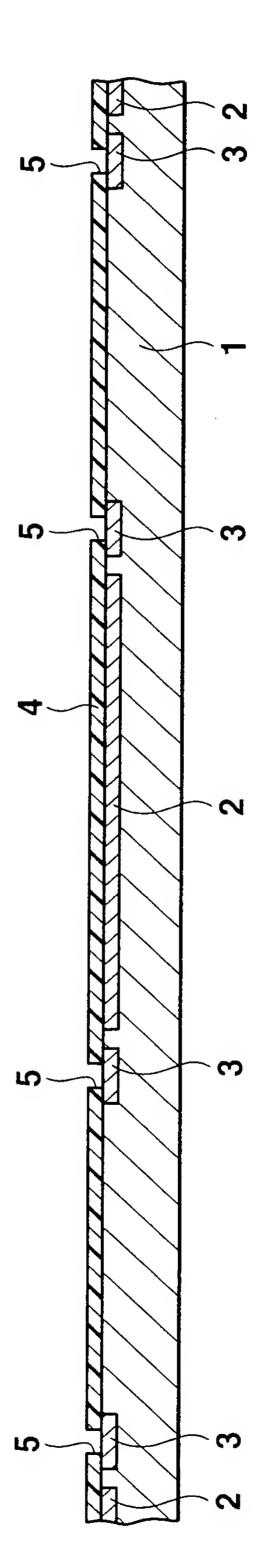
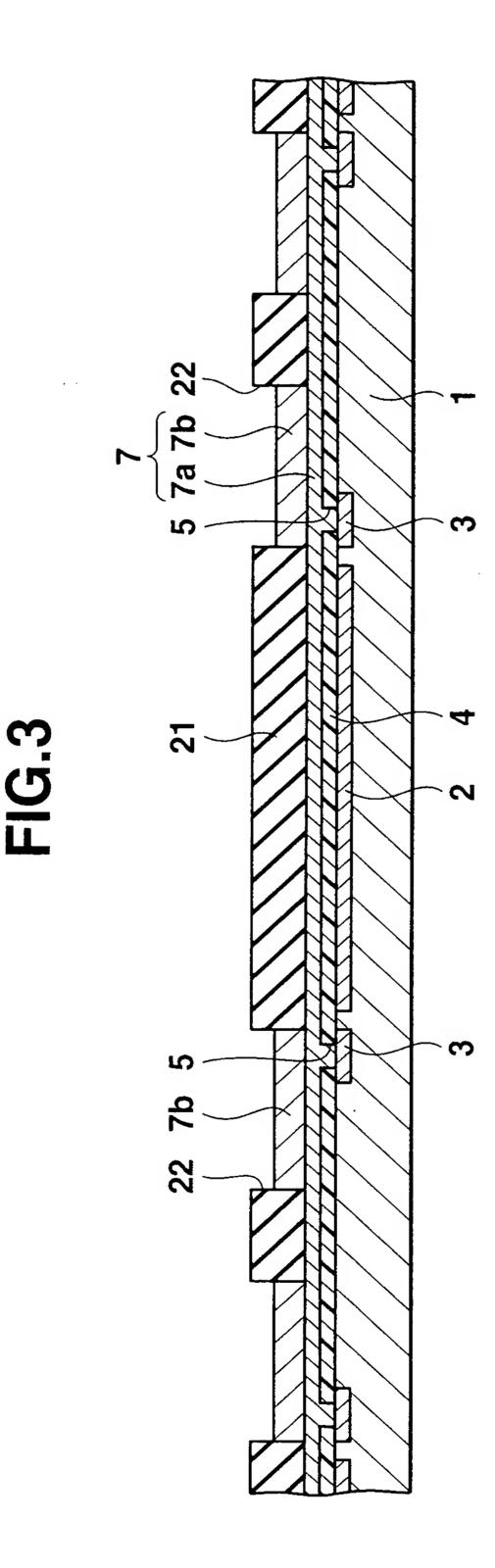
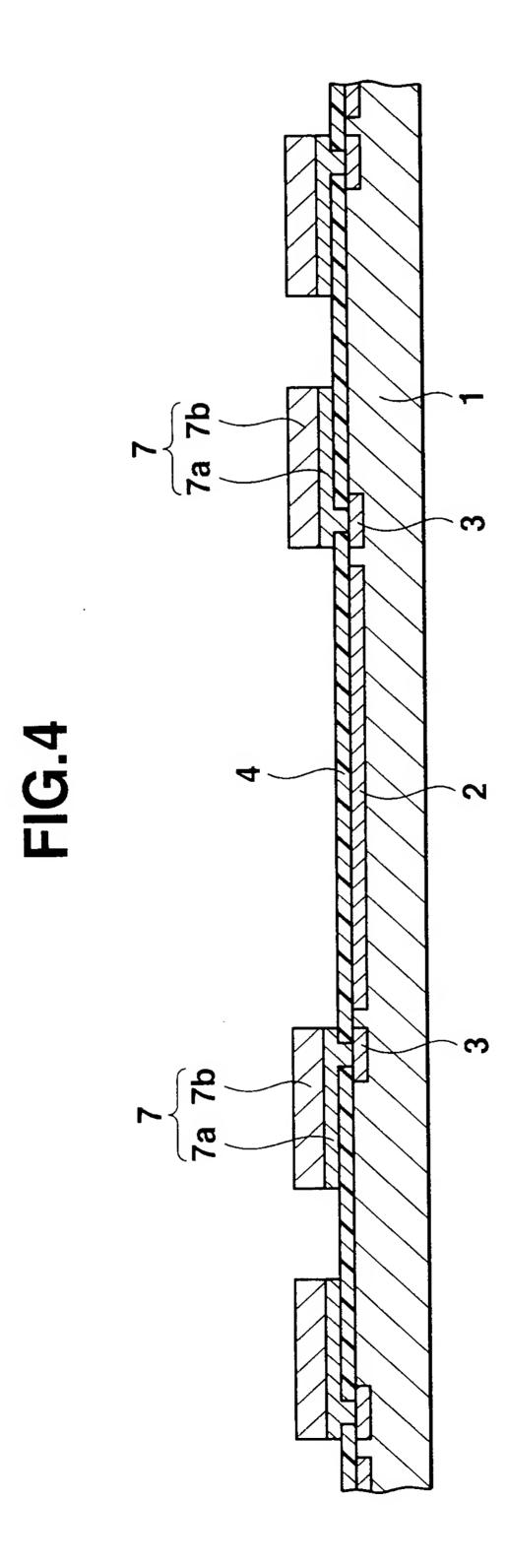


FIG.2







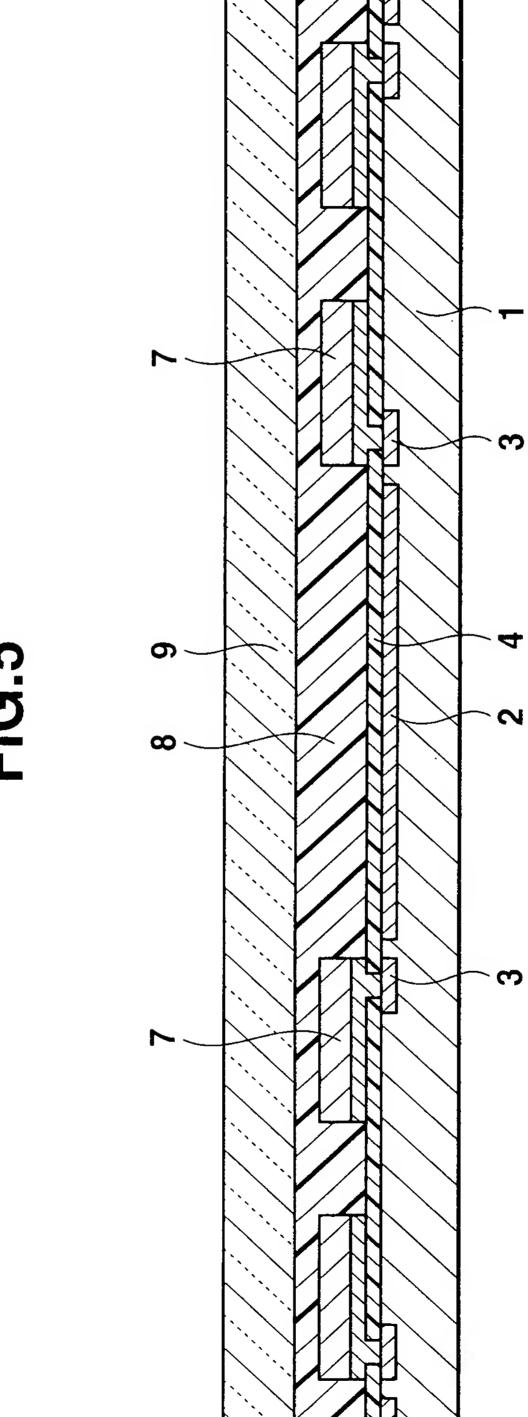


FIG.5

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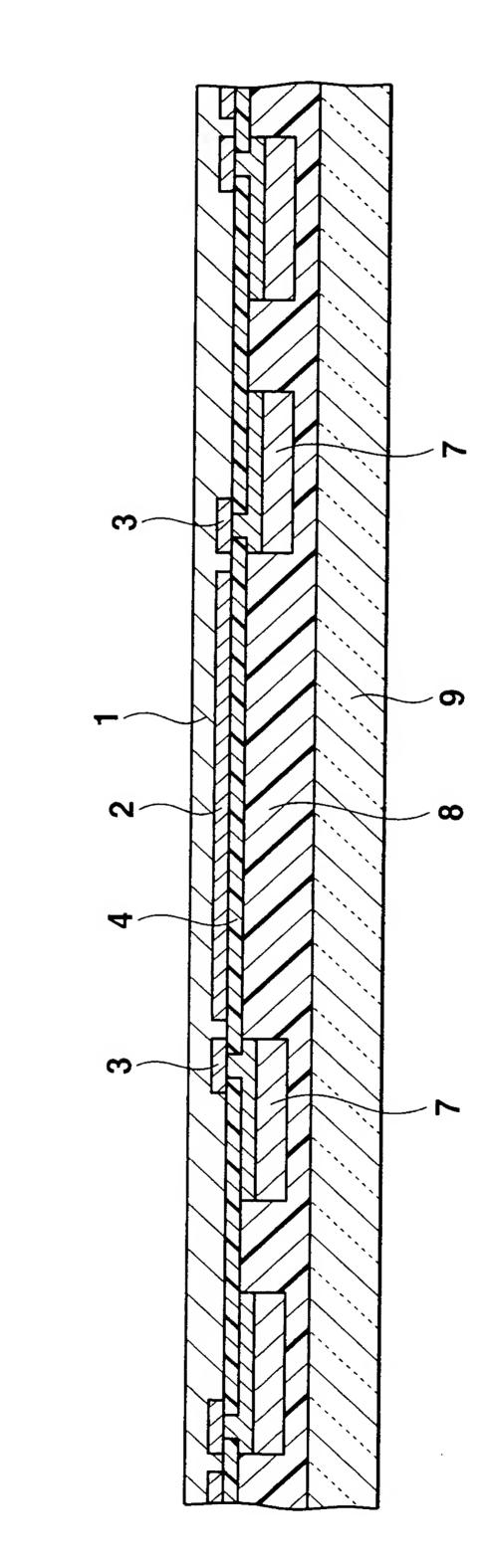


FIG.6

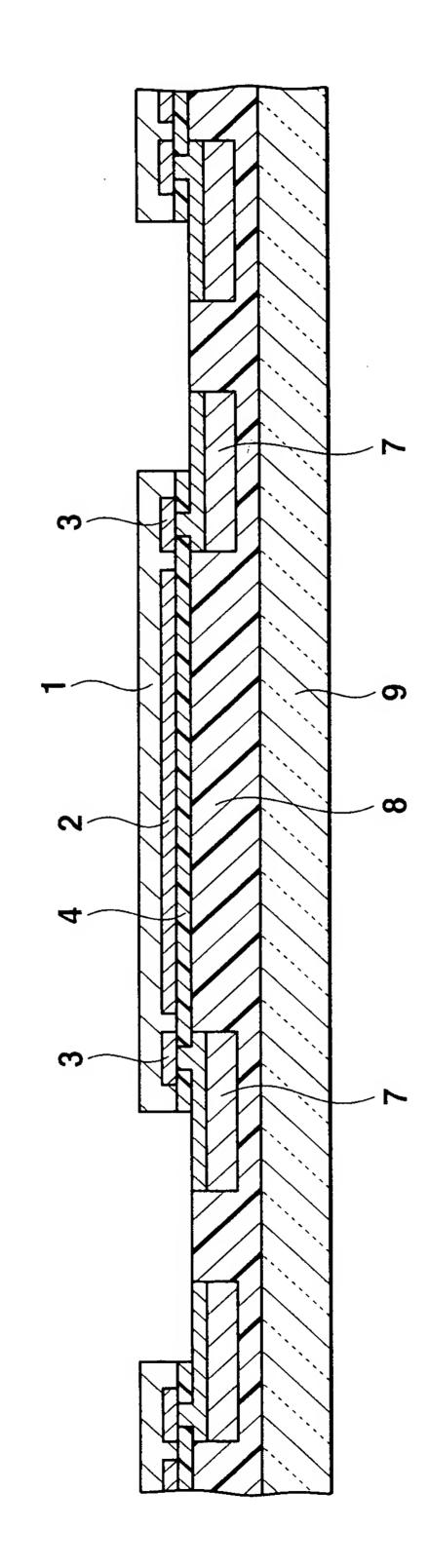


FIG.7

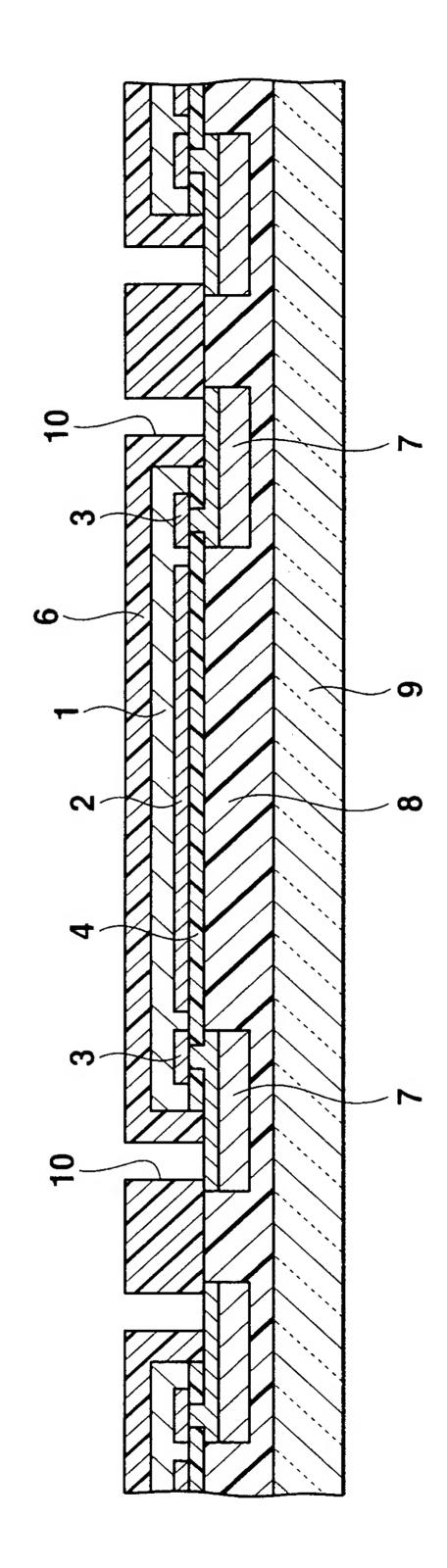
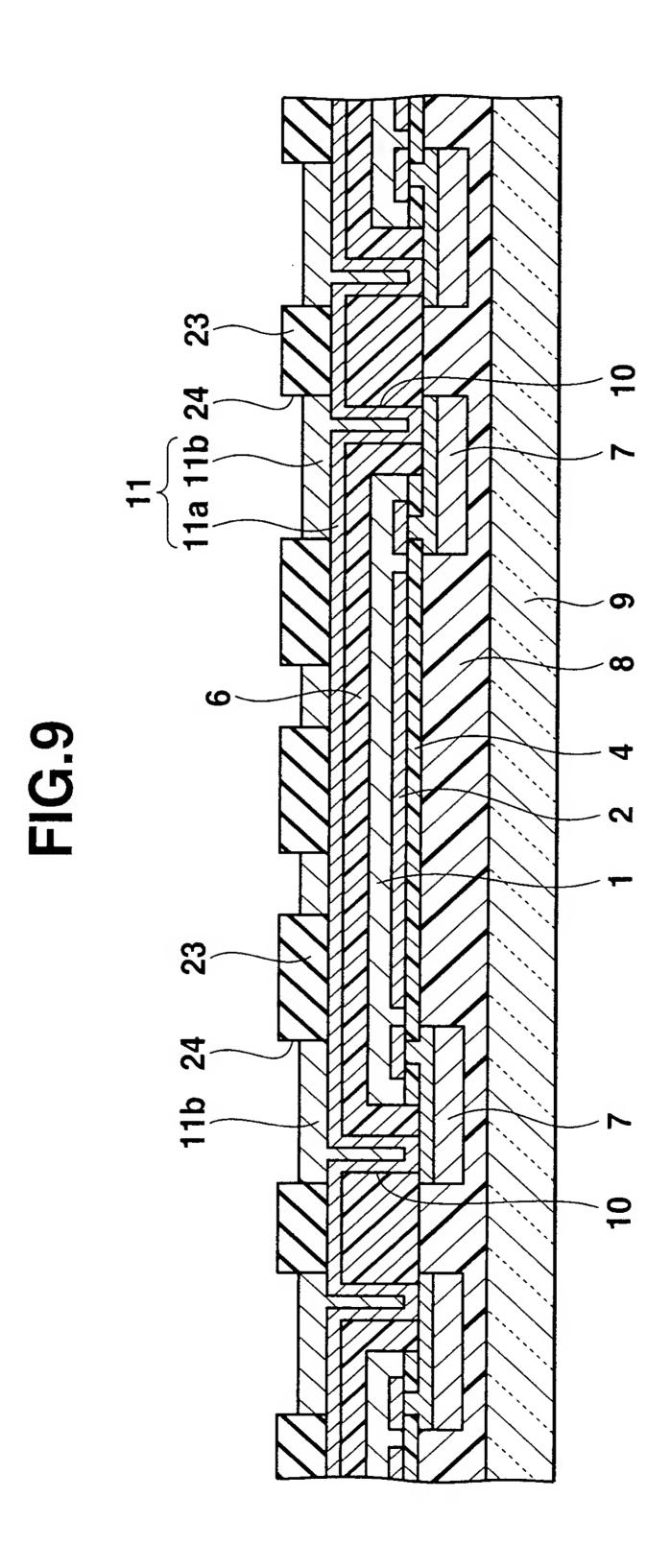
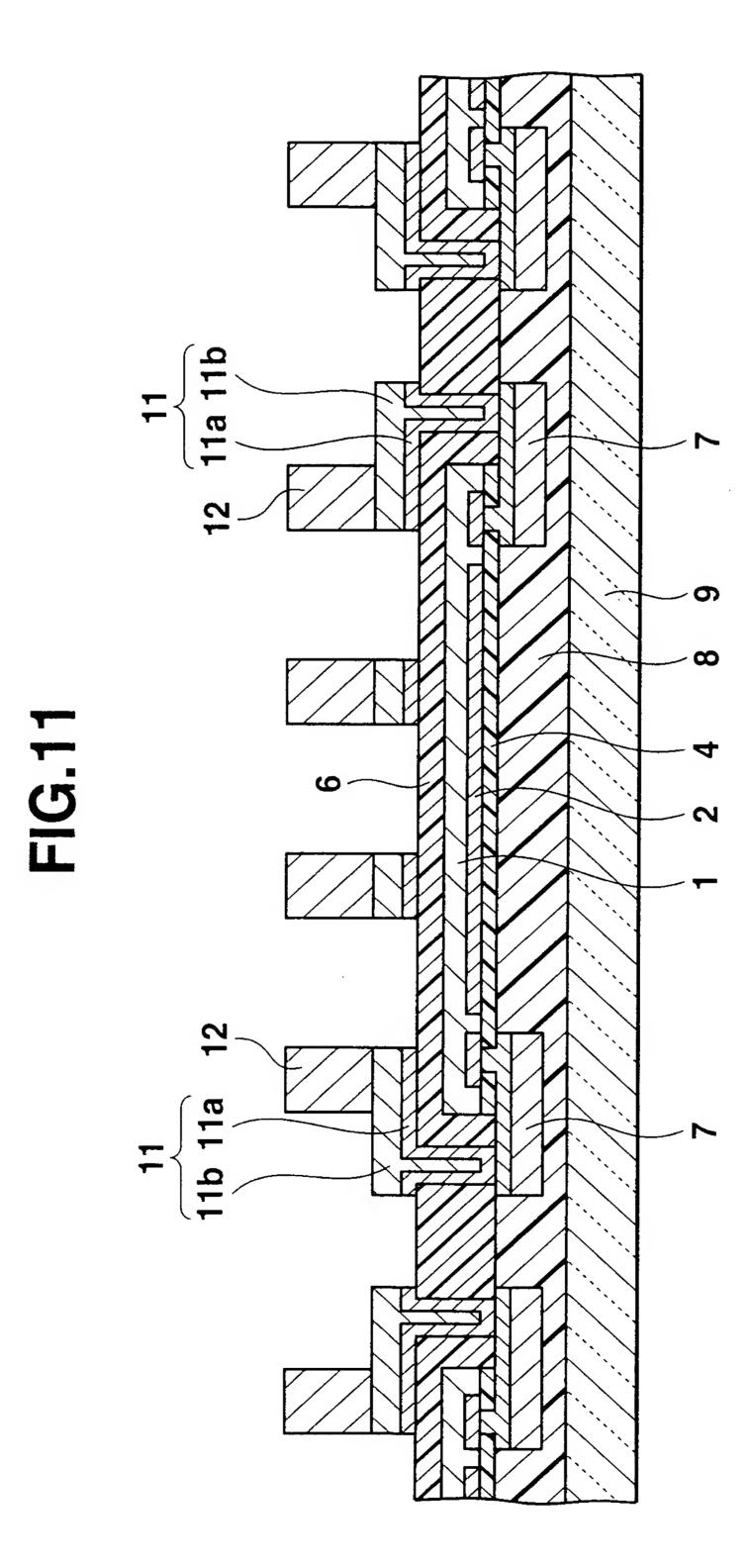


FIG.8



52 12 26 11b 11a 6 ∞ 25 **- 9** 12 26 11b

FIG.10



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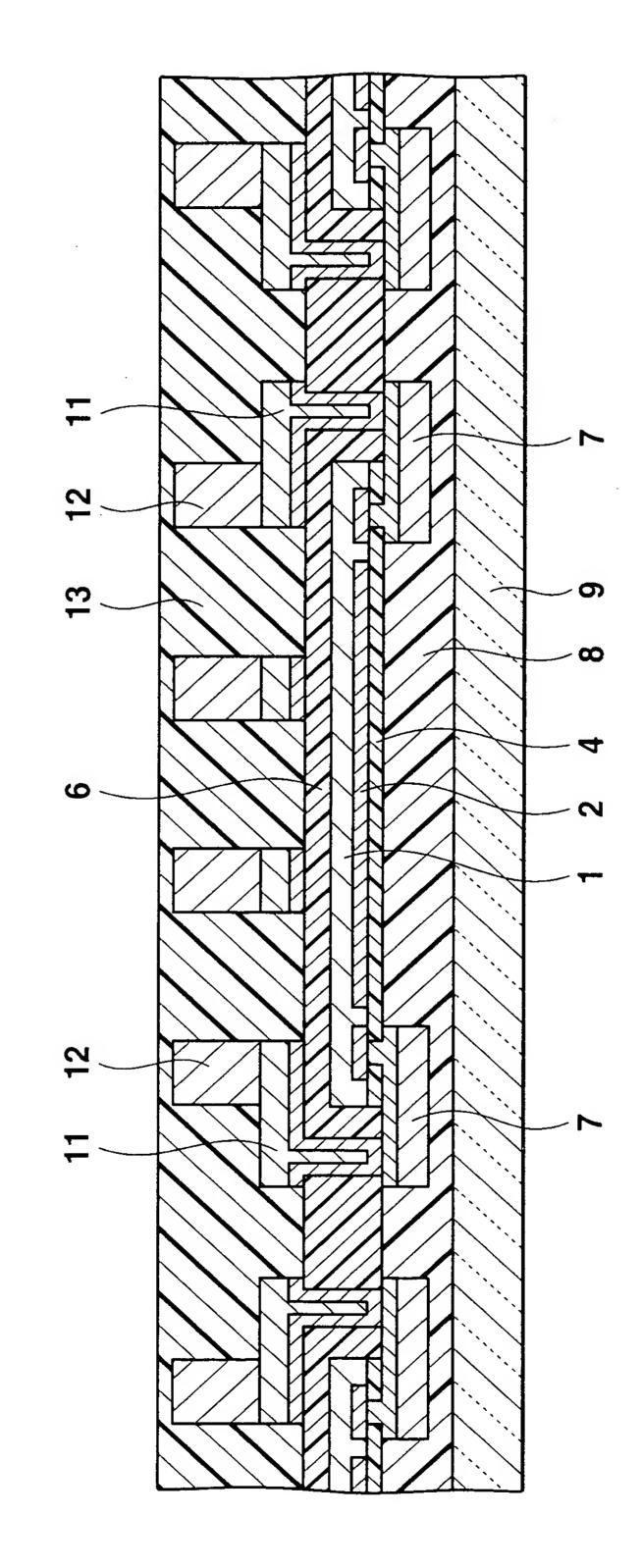


FIG.12

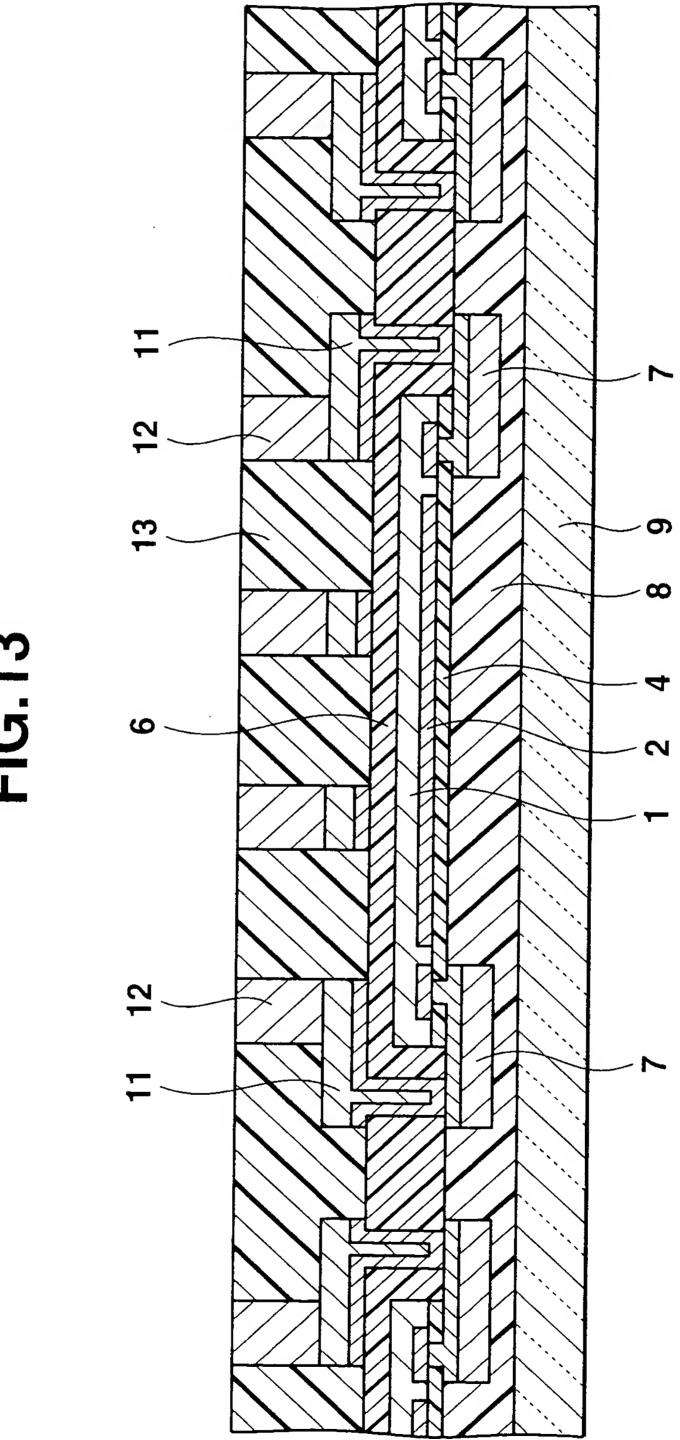


FIG.13

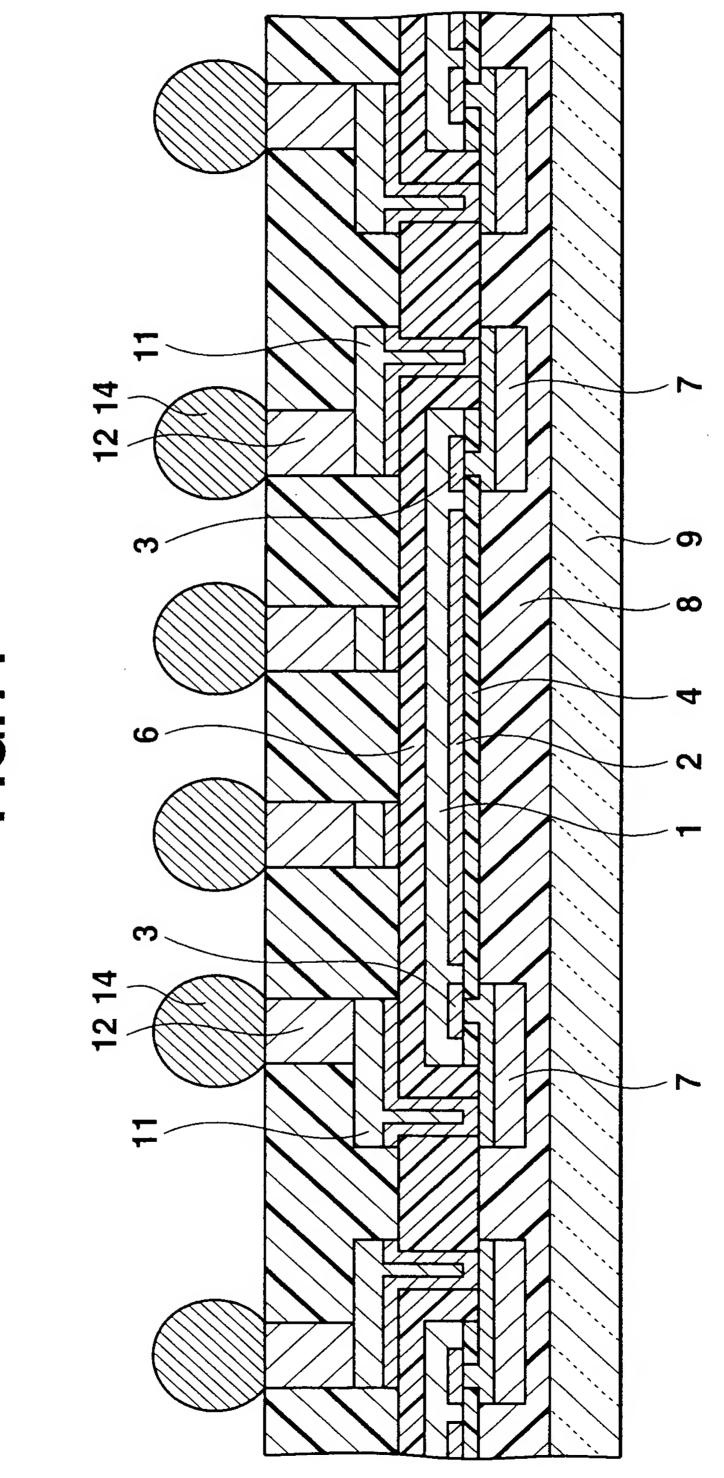
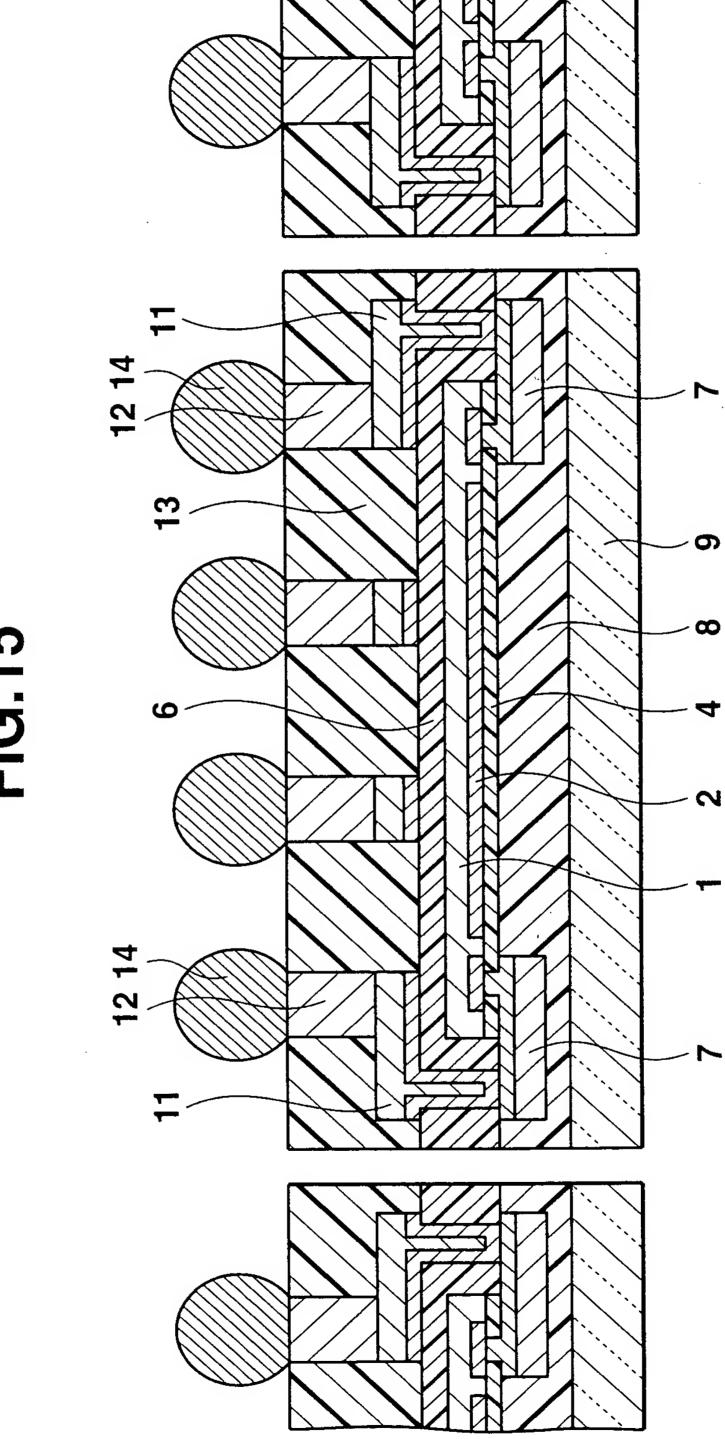


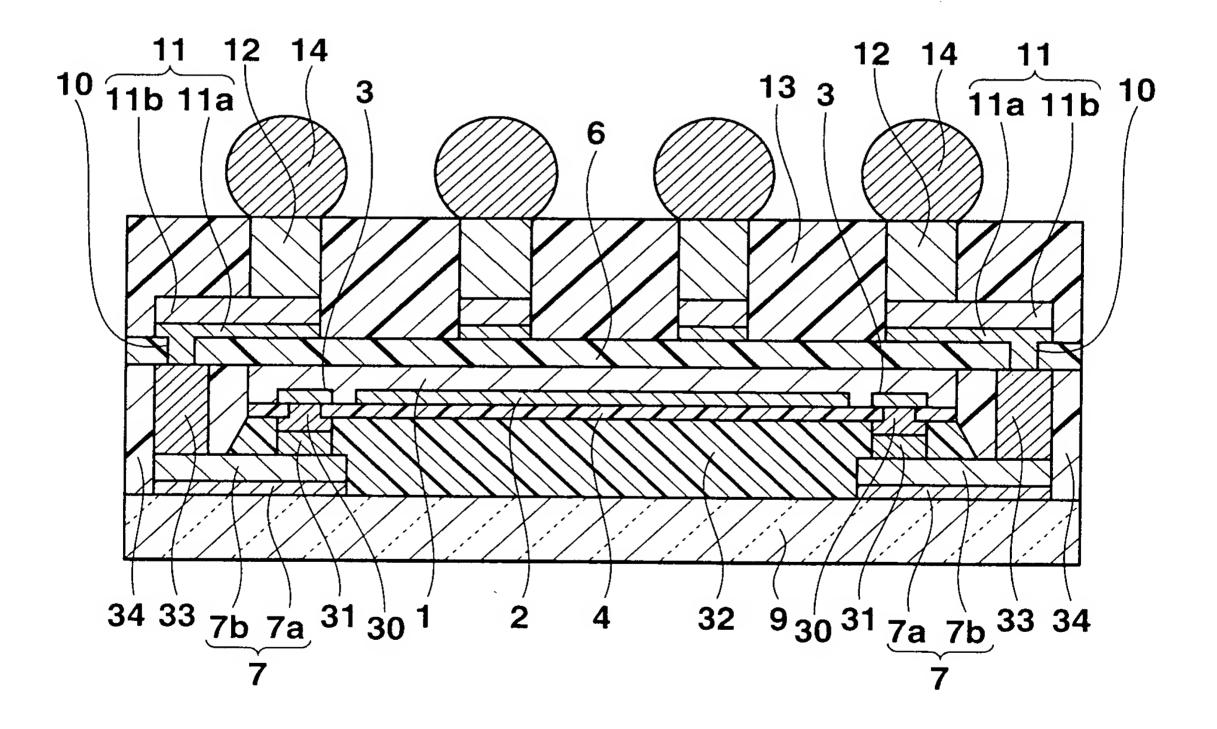
FIG.14



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FIG.15

FIG.16



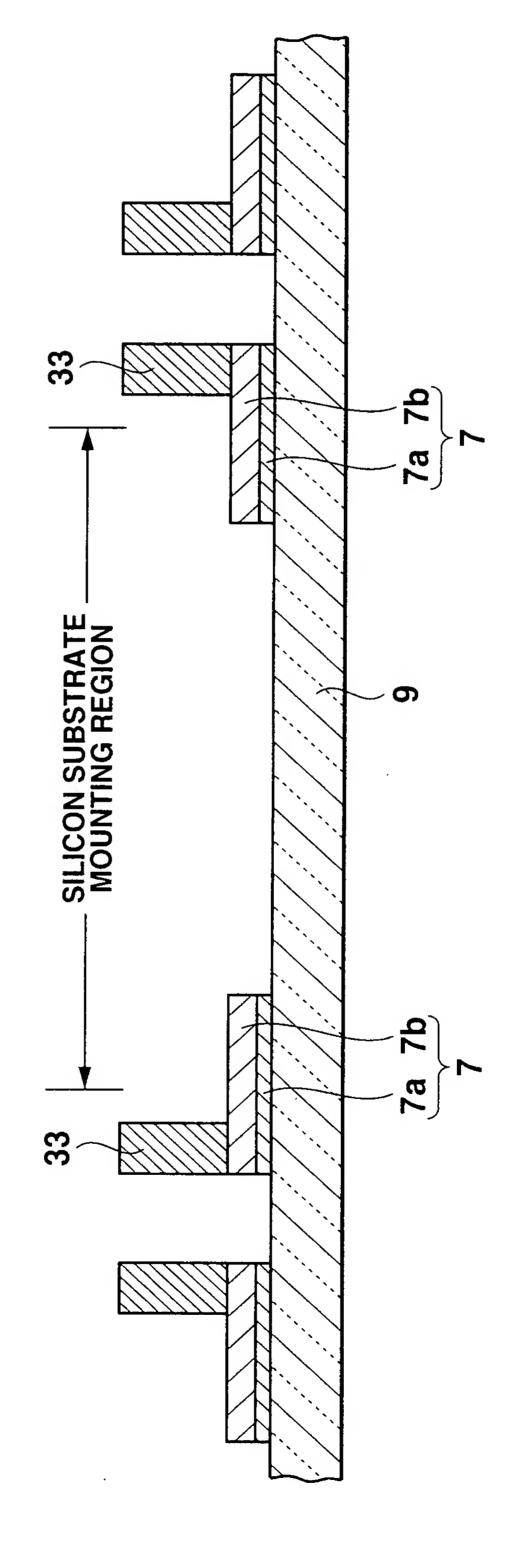


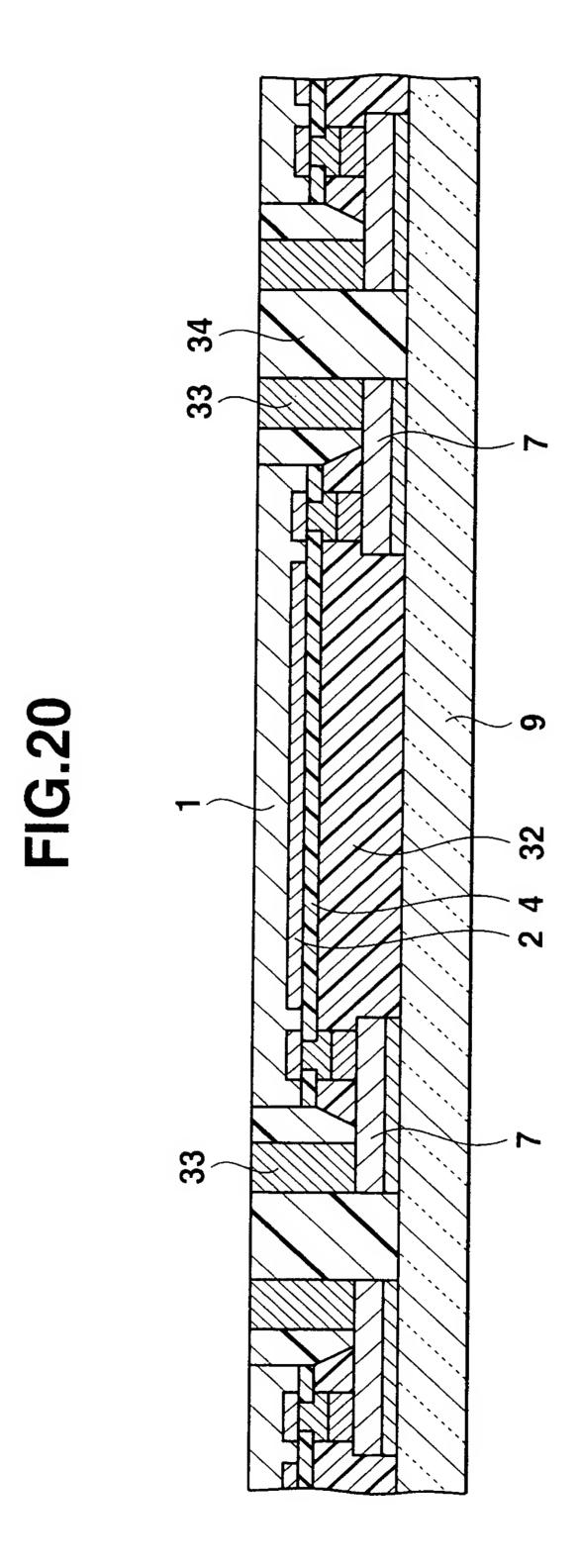
FIG.17

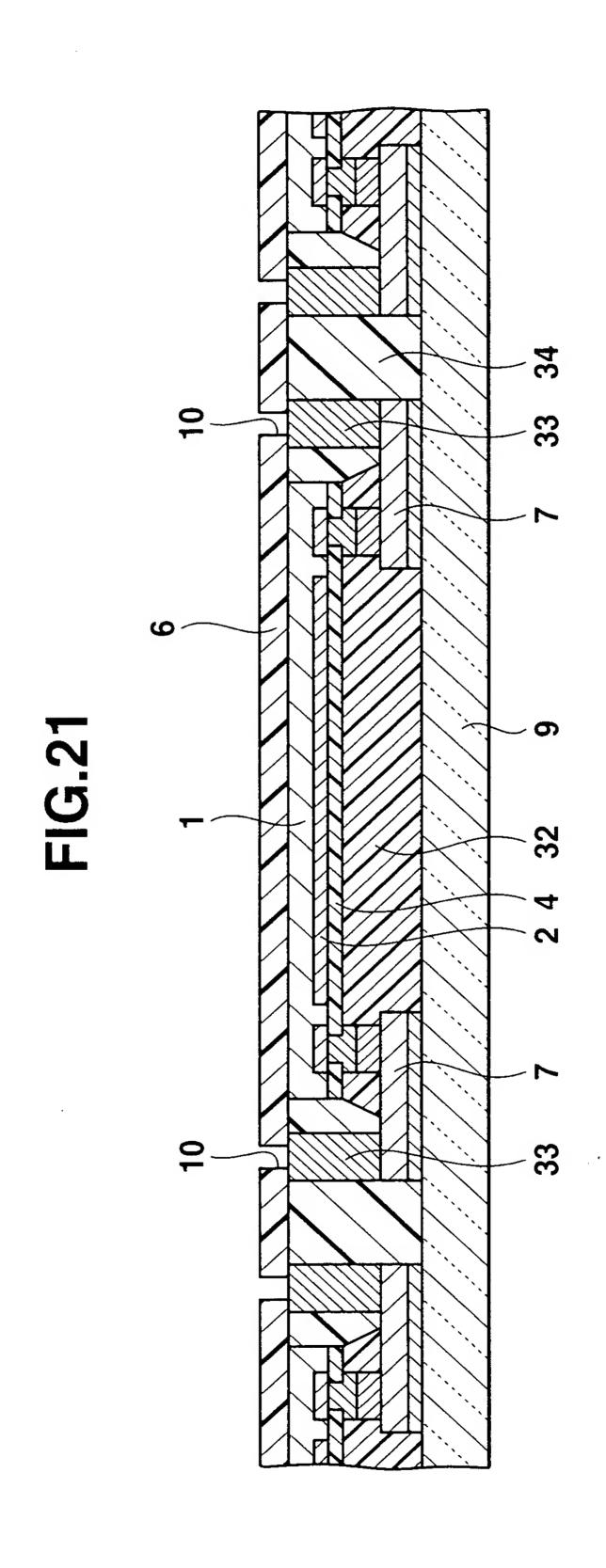
SILICON SUBSTRATE MOUNTING REGION

FIG. 18

FIG. 19

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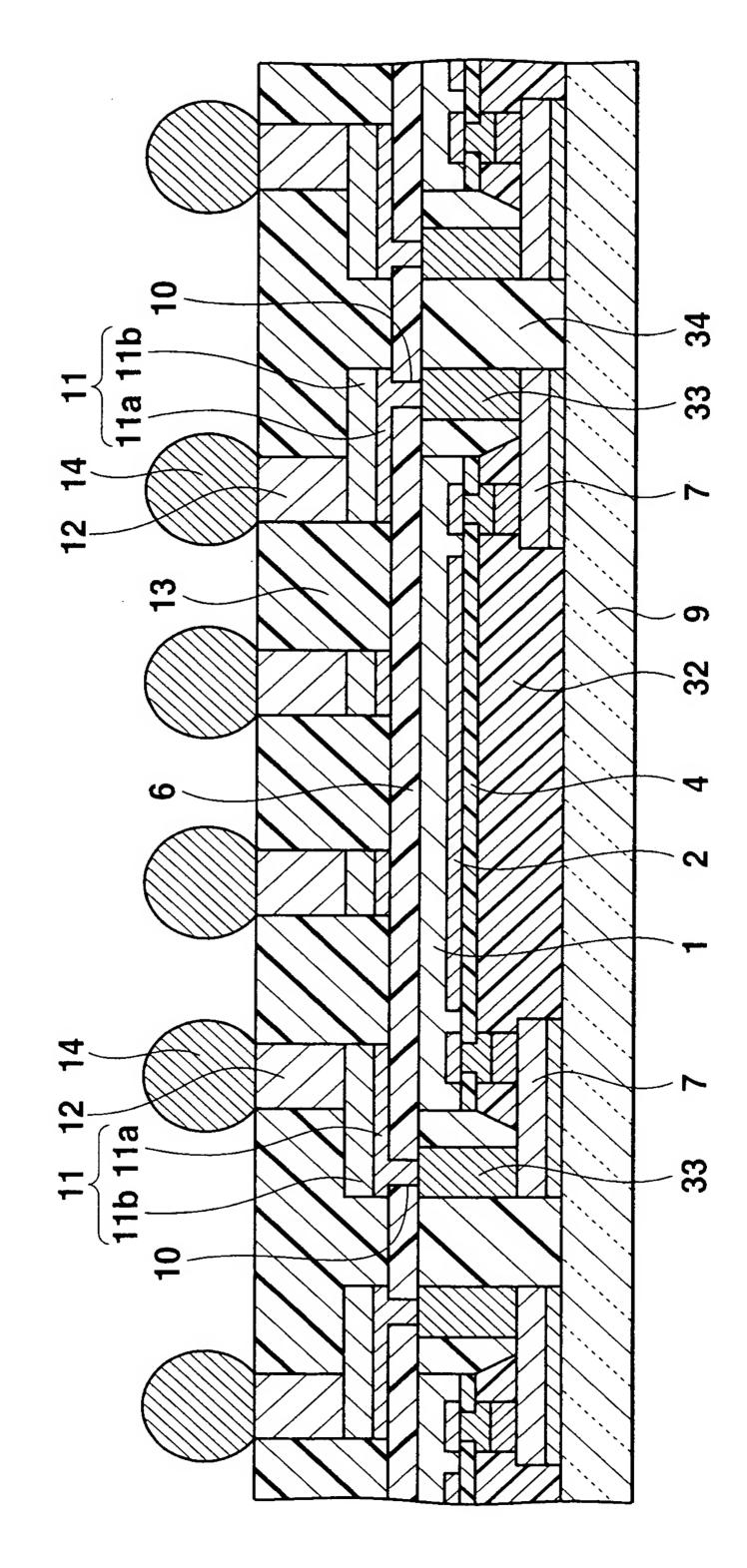


FIG.22

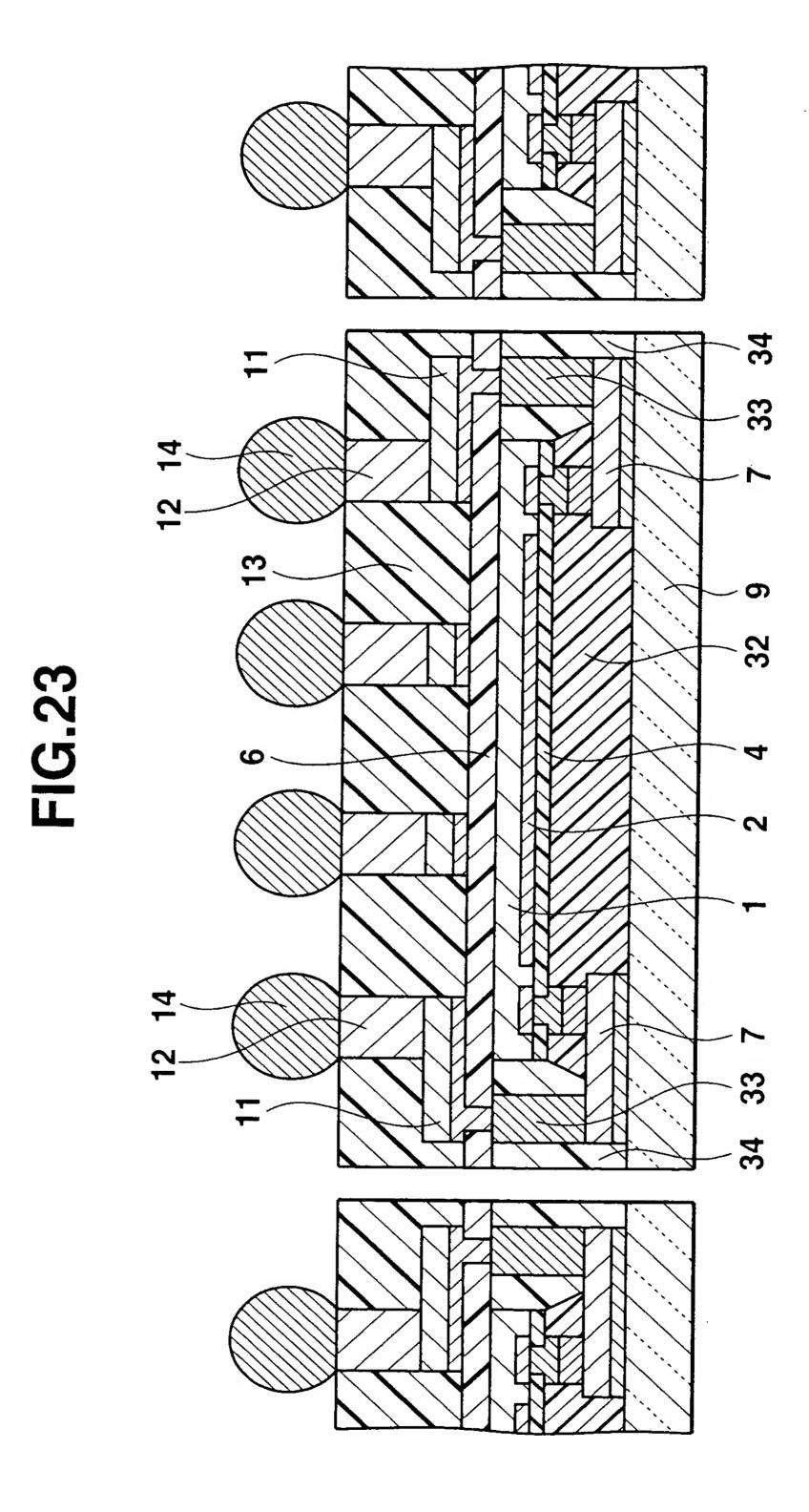


FIG.24

